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Request for grant of a patent

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1. Your reference
Active layer island-150103

2. Patent application number
(The Patent Office will fill in this part)
0301089.9
17 JAN 2003

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*
Plastic Logic Limited
34 Cambridge Science Park
Cambridge CB4 0FX

8184533001

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation
UK

4. Title of the invention
Active layer islands

5. Name of your agent *(if you have one)*
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London WC1N 2LS

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

Patents ADP number *(if you know it)*
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Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*
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Claim *(s)*	5
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11. I/We request the grant of a patent on the basis of this application.

Signature H. Sirringhaus Date 15.01.03

12. Name and daytime telephone number of person to contact in the United Kingdom H. Sirringhaus 01223 706 002

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ACTIVE LAYER ISLAND

This invention relates to solution processed devices and methods for forming such devices.

Semiconducting conjugated polymer thin-film transistors (TFTs) have recently become of interest for applications in cheap, logic circuits integrated on plastic substrates (C. Drury, et al., APL 73, 108 (1998)) and optoelectronic integrated devices and pixel transistor switches in high-resolution active-matrix displays (H. Sirringhaus, et al., Science 280, 1741 (1998), A. Dodabalapur, et al. Appl. Phys. Lett. 73, 142 (1998)). In test device configurations with a polymer semiconductor and inorganic metal electrodes and gate dielectric layers high-performance TFTs have been demonstrated. Charge carrier mobilities up to 0.1 cm^2/Vs and ON-OFF current ratios of 10^6-10^8 have been reached, which is comparable to the performance of amorphous silicon TFTs (H. Sirringhaus, et al., Advances in Solid State Physics 39, 101 (1999)).

Thin, device-quality films of conjugated polymer semiconductors can be formed by coating a solution of the polymer in an organic solvent onto the substrate. The technology is therefore ideally suited for cheap, large-area solution processing compatible with flexible, plastic substrates. To make full use of the potential cost and ease of processing advantages it is desirable that all components of the devices including the semiconducting layers, the dielectric layers as well as the conducting electrodes and interconnects are deposited from solution.

To fabricate all-polymer TFT devices and circuits the following main problems have to be overcome:

- Integrity of multilayer structure: During solution deposition of subsequent semiconducting, insulating and/or conducting layers the underlying layers should not be dissolved, or swelled by the solvent used for the deposition of

the subsequent layers. Swelling occurs if solvent is incorporated into the underlying layer which usually results in a degradation of the properties of the layer.

- High-resolution patterning of electrodes: The conducting layers need to be patterned to form well-defined interconnects and TFT channels with channel lengths $L \leq 10\mu m$.
- To fabricate TFT circuits vertical interconnect areas (via holes) need to be formed to electrically connect electrodes in different layers of the device.

In PCT/GB00/04934 a method is described by which high performance transistors with well-defined and controlled channel lengths of less than 10 μm can be fabricated by solution processing in combination with direct printing. The method (see Fig.1) is based on patterning the surface energy of the substrate 1 into high surface energy, hydrophilic regions 3 and low-surface energy, hydrophobic regions 2 . When ink droplets of a conducting ink 4, such as of the conducting polymer polyethylenedioxythiophene doped with polystyrene sulfonic acid (PEDOT/PSS) are deposited into the high surface energy regions, the droplets spread inside the hydrophilic region, but their spreading is confined when they hit the hydrophobic barriers (Fig. 1B). Alternatively, the droplets can also be deposited directly on top of the hydrophobic barrier region defining the channel length L. If the surface energy of the barrier region is sufficiently low, the ink droplets split in half, and deposit on each side of the barrier. In some situation this process is advantageous compared to the one described in Fig. 1B. For a given droplet volume the minimum width of the source and drain electrodes can be lower by up to a factor 2, because the total ink volume splits in half, and each side of the channel barrier contains only half as much ink than if source and drain areas were filled separately. This process results in formation of source and drain electrodes 5 with very high resolution. Devices are completed by deposition of a continuous or patterned semiconducting active layer 6, a gate dielectric layer 7, and finally a gate electrode 8.

For many applications the active semiconducting layer needs to be patterned into an active layer island. This is necessary in order to reduce electrical crosstalk and eliminate parasitic leakage currents between neighbouring devices. Even if the semiconducting material is not doped, leakage currents through the semiconducting layer can be significant, in particular for circuits with a high packing density of transistors, such as high resolution active matrix displays. In an active matrix display metallic interconnects are running for pixel addressing are running across the display. If semiconducting material is present underneath such interconnects lines, parasitic TFT channels can form underneath these interconnect lines, giving rise to non-negligible leakage currents between pixels.

Patterning of a semiconductor active layer island can be achieved by inkjet printing of an ink of the semiconducting material on top of the predeposited source-drain array (Fig. 1C). Ideally, in applications where integration density is to be maximised, the active layer island should not be much larger than the source-drain electrode pattern. For many inks this is not easy to achieve. Inks for semiconducting material, such as conjugated polymer semiconductors, are often formulated in highly non-polar solvents, such as xylene, or mesitylene. These solvents have low surface energies, i.e., on wetting substrates droplets of such non-polar ink formulations spread to a large diameter of typically 50-200 μm diameter for typical inkjet droplet volumes of 10 – 50 pl. On the other hand, inks for conducting materials, such as PEDOT/PSS in water tend to be formulated in more polar, high surface energy solvents, that spread significantly less. In many situations, the diameter of a dried non-polar semiconducting droplet is significantly larger than the combined width of the source and drain electrodes.

In many applications there is less need for patterning of the gate dielectric layer. A continuous layer of gate dielectric deposited, for example, by processes such as blade, spin, spray or extrusion coating can be useful to allow crossing of interconnects at the source-drain and gate level without the need for deposition of

additional insulation layers. However, in the case of unpatterned gate dielectric layers via-hole interconnections are required whenever electrical connections between electrodes / interconnects in a top layer need to be connected electrically to electrode / interconnects in a bottom layer. If the dielectric layer is patterned, however, such connections can simply be established by printing over the edge of the dielectric pattern (PCT/GB00/04942).

According to a first aspect of the present invention there is provided device(s) and method(s) as set out in the accompanying independent claims. Preferred features are set out in the dependant claims.

According to one aspect of the present invention there is provided a method by which a same surface energy pattern is used for the confinement of a solution of a first material, and subsequently the same surface energy pattern is used for the confinement of a solution of at least one additional material.

According to another aspect of the present invention methods are provided that prevent dewetting of the solution of the additional material from certain narrow features of the surface energy pattern, from which the solution of the first material dewets.

The invention enables fabrication of self-aligned active layer islands for solution-processed, and directly printed TFTs.

The present invention will now be described by way of example, with reference to the accompanying drawings, in which:

figure 1 shows the use of a surface energy pattern for the printing of source-drain electrodes of a TFT with high resolution.

figure 2 shows a method by which the same surface energy pattern that is used for the confinement of the ink for source and drain electrodes is also used for the definition of an active layer island of the TFT.

figure 3 shows top-view drawings of various designs for the surface energy pattern designed to discourage dewetting of the active layer semiconductor in the region of the channel.

figure 4 shows different drying modes of the semiconducting solution.

figure 5 shows methods by which electrical interconnects to the gate electrode can be formed in the case of a patterned dielectric layer.

The invention will now be described with reference to Fig. 2. As in PCT/GB00/04934 the process starts with the definition of a surface energy pattern that creates regions of high surface energy 10, and low surface energy 11 and 12 on the substrate 9. Region 12 defines the channel length of the transistor device, region 11 confines the solution for the deposition of source and drain electrode to a form source and drain electrodes 13 with a narrow linewidth. The solution for the conducting source-drain electrodes can be deposited by a range of different printing techniques including, but not limited to, inkjet printing, soft lithographic printing (J.A. Rogers et al., Appl. Phys. Lett. 75, 1010 (1999); S. Brittain et al., Physics World May 1998, p. 31), screen printing (Z. Bao, et al., Chem. Mat. 9, 12999 (1997)), and photolithographic patterning (see WO 99/10939), offset printing, spin-coating, blade coating or dip coating, curtain coating, meniscus coating, spray coating, extrusion coating. A preferred technique is drop-on demand inkjet printing.

Subsequently, a solution of the active semiconducting material 14 is deposited from solution. For the deposition of the semiconducting material also a broad range of printing techniques can be used including, but not limited to, inkjet printing, soft lithographic printing (J.A. Rogers et al., Appl. Phys. Lett. 75, 1010 (1999); S. Brittain et al., Physics World May 1998, p. 31), screen printing (Z.

Bao, et al., Chem. Mat. 9, 12999 (1997)), and photolithographic patterning (see WO 99/10939), offset printing, spin-coating, blade coating or dip coating, curtain coating, meniscus coating, spray coating, extrusion coating. Also here, a preferred technique is drop-on demand inkjet printing.

The ink formulation and the surface wetting conditions prior to deposition of the semiconducting ink are chosen such that

a) The solution of the semiconducting material is repelled by the low energy surface region 11, and upon drying of the solvent of the solution no deposition of semiconductor occurs on top of region 11.
b) The solution of the semiconducting material does not dewet from the low energy surface region 12, and after drying of the solvent forms an essentially continuous film over the channel region 12, that is also in contact with the source and drain electrodes.

It is a key feature of the invention that the semiconducting ink is repelled by surface region 11, but does not dewet from surface region 12. Whereas many conducting materials can be formulated in relatively polar solvents with high surface energies, many semiconducting inks, such as those for many conjugated polymer, those of polyalkylthiophene or polyfluorene based semiconducting polymers, need to be formulated in non-polar solvents such as xylene or mesitylene. These solvents have a low surface energy.

It can be shown (see H. Sirringhaus, et al., MRS Bulletin July 2001, page 539) that the repulsive force that is acting on a liquid droplet spreading in a surface region of high surface energy, and then coming in contact with a surface region of low surface energy is proportional to the surface tension, and to the difference between the dynamic contact angle on the high energy surface $\theta(R_s)$ and the contact angle on the low energy surface θ_p.

$$F_s = \lambda_{LV}\left(cos\,\theta(R_s) - cos\,\theta_p\right)$$

Therefore it is generally more difficult to confine a low-surface energy ink by a surface energy pattern than a high surface-energy ink, i.e. in many cases the surface energy pattern on the substrate is be able to confine the polar conducting ink to region 10, but the subsequently deposited semiconducting ink will not be sufficiently repelled by the surface region 11. In order to confine a low-surface energy ink, the surface region 11 needs to exhibit a contact angle for the semiconducting ink that is significantly higher than that on the surface of the conducting ink 13. Preferably the difference in contact angle between the two regions is higher than 10°, more preferably higher than 30°.

Various techniques can be used to produce surface barrier layers that produce a high contact angle for non-polar semiconducting inks. In one preferred embodiment of the invention the surface of the substrate is fluorinated in regions 12 and 11. A fluorinated surface has a lower surface energy than most common non-polar solvent inks, and is therefore capable of confining both the polar conducting ink and the nonpolar semiconducting ink. Selective fluorination of the substrate surface can be achieved in a range of different ways:

- Deposition of a layer of polymer, such as hydrophobic polyimide onto a glass substrate 9, followed by patterning of the polymer as to define opening regions 10 where the bare substrate is exposed. Then the substrate is exposed to a plasma treatment of CF_4 or other fluorinated gaseous species. CF_4 selectively fluorinates the surface of the polymer, but does not modify the surface properties of the glass substrate to the same degree. The patterning of the polymer can be achieved, for example, by photolithographic patterning, thermal transfer printing or direct write exposure to a focussed light beam (UK 0116174.4).

- Deposition of a fluorinated self-assembling monolayer (SAM) molecule, such as a fluorinated tri-/ di-/ mono-chlorosilane, or tri-/ di-/ mono-alkoxysilane, onto a substrate to which the monolayer can form a covalent bond. Patterning of the SAM molecule can be achieved by techniques such as, but not limited to, soft lithographic stamping, photolithography, exposure to focussed light beams, or embossing of the substrate followed by contact with a flat stamp inked with the SAM molecule.

It is a preferred embodiment of the invention that the surface energy pattern used for the confinement of the semiconducting ink is essentially the same surface energy pattern that is responsible for the confinement of the conducting ink. However, after deposition of the conducting source and drain electrodes and prior to the deposition of the semiconducting material the substrate may be subject to a surface treatment step in order to control the wetting conditions of the semiconducting ink on the various surface regions 13, 12, 11, and possibly uncovered surface regions 10. This surface treatment might selectively increase the surface energy of the conductive material. This surface treatment might also involve a patterning or masking step by which some regions are protected during such surface treatment step. However, preferrably there is no additional patterning step associated with such surface treatment.

An alternative technique to achieve confinement of the semiconducting ink is to make use of surface roughness effects. On a microscopically rough surface the contact line of a spreading droplet is easily pinned. When a droplet of semiconducting ink hits a microscopically rough surface region 11, spreading comes to a halt, and the contact lines becomes pinned at the boundary of regions 11 and 10/13. The surface roughness effect can also be used in combination with a surface energy contrast in order to enhance the ability of region 11 to confine the incoming droplet.

The microscopic surface roughness can be generated by a range of techniques such as, but not limited to:

- Physical or chemical etching of a patterned layer deposited onto the substrate: The layer may have more than one component, with one component having a higher etch rate than the other components. An example of such a material would be a patterned layer of blend of two or more polymers, where one of the polymers can be dissolved selectively by exposing the layer to a solvent in which the other polymer(s) is (are) not soluble or are only poorly soluble.
- Embossing of a surface layer : A soft layer of polymer patterned on top of a more rigid substrate can be embossed with an embossing tool containing a high density of sharp protruding structure that define an array of topographic features such as linear grooves or pits in the polymer layer.
- Bombardment of a substrate containing a patterned surface layer with ions, such as sputtering with Argon ions.
- Exposure of the substrate to light either through a shadow mask or using a focussed light beam scanned across the surface.
- Mechanical rubbing of the substrate.
- Annealing of the substrate.

It is another key feature of the invention that the semiconducting ink in spite of being repelled from surface region 11 does not dewet from surface region 12 (in contrast to the ink of the conducting material). In one embodiment of the invention this is achieved by controlling the surface energies of regions 11 and 12 separately, i.e. by preparing surface region 12 in a state with slightly higher surface energy than region 11. Of course the surface energy of region 12 always needs to be low enough as to repel the ink of the conducting material. However, such a process usually requires a separate patterning step in order to define the differential surface energy contrast between regions 12 and 11. Preferably, dewetting of the semiconducting ink from region 12 is avoided without a surface

energy contrast between regions 11 and 12, i.e. , without an additional patterning step.

In order to prevent dewetting from region 12 it is also preferred that the semiconducting ink is deposited directly on top of region 12, as opposed to being deposited into region 13.

Below we list several different embodiments of the invention by which dewetting can be prevented:

- Control of surface tension of the semiconducting ink: In order to be effectively repelled by region 11 the surface tension of the semiconducting ink needs to be higher than a critical value γ_{LV}^{min}, that depends on the surface conditions of the substrate, the deposition conditions of the ink, and environmental factors such as temperature. In order for the semiconducting ink not to dewet on top of region 12, its surface tension needs to be lower than a critical value γ_{LV}^{max}. γ_{LV}^{min}, and γ_{LV}^{max} can be determined experimentally by systematic variation of the surface tension. The surface tension can be controlled, for example, by choice of solvents, the addition of a cosolvent or addition of a surfactant. In the range of surface tensions $\gamma_{LV}^{min} < \gamma_{LV} < \gamma_{LV}^{max}$ confined & continuous active layer island can be deposited.

- Control of surface tension of substrate: Similarly, the surface tension of the substrate γ_{SV} in region 12 and 11 (assumed here to be of identical surface composition) can be controlled such that $\gamma_{SV}^{min} < \gamma_{SV} < \gamma_{SV}^{max}$, where γ_{SV}^{max} is the maximum surface tension that still provides efficient repulsion of the inks of both the conducting and the semiconducting material from region 11. γ_{SV}^{min} is the minimum surface below which dewetting of the ink occurs on region 12. The substrate surface tension can be varied, for example, by altering the chemical composition of the substrate, or by exposing the substrate to a

surface treatment or electromagnetic radiation, or by controlling the temperature and humidity conditions before and during the deposition.

- Increasing viscosity of the semiconducting ink: A high solution viscosity facilitates ink confinement, as it reduces the kinetic energy of the contact line of the spreading droplet. A high viscosity also prevents dewetting on top of region 12, because it reduces the mobility and flow of molecules in solution that is required to split one droplet into several separate isolated droplets. The viscosity can also be controlled by judicious choice of solvents, addition of cosolvents, or by increasing the concentration and / or molecular weight of a semiconducting polymer in solution, or by lowering of the solution temperature.

- Decreasing drying time: The dewetting process occurs on a different time scale than the ink confinement process. During the initial fast spreading of the droplet the solution covers the whole of area 13 and 12, and is repelled from region 11. Dewetting tends to occurs on a longer time scale during the drying of the solution. If the solution is formulated in a low boiling point solvent or if the evaporation rate of the solvent is enhanced, for example by depositing onto a heated substrate, exposing the substrate to electromagnetic radiation during deposition and drying, or by depositing under a flow of "dry", inert gas, the drying time is decreased. The viscosity of the solution increases rapidly during drying, and by the time dewetting would occur, the solution viscosity is already so high that dewetting is suppressed.

- Controlling the print sequence and the total volume of liquid : In the case of inkjet deposition the amount of liquid that is deposited can be controlled by the ejection frequency, the drive conditions the inkjet head, and by the speed at which the sample is moving underneath the printhead. By reducing the total volume, and printing in such a way that each droplet of semiconducting is partially dried before it comes into contact with another droplet landing on the

substrate, one can avoid buildup of liquid ink, that takes a long time to dry, and is prone to exhibit dewetting. Interleaved printing where isolated droplets are printed in a first pass, and the gaps between the droplets are filled in during subsequent passes, can be used to achieve this.

- Design of surface energy pattern : The surface energy pattern can be designed in such a way that at the edges of region 12 areas of high surface energy 10 are incorporated that are not covered by conducting material, but fix (pin) the contact line of the semiconducting ink. Once the contact line is pinned, i.e. semiconducting material starts to dry at the edge of the still liquid droplet, the tendency of the droplet to dewet is much suppressed. Illustrative examples for possible pattern design as shown in Fig. 3. In Fig. 3A the whole of surface region 10 is filled with conductive material. During deposition of the semiconducting ink, the droplets have a tendency to dewet and split into two droplets starting at the two boundary regions where regions 12 and 11 meet. This can be avoided by the design illustrated in Fig. 3B or Fig 3C, which replace the direct link between low-surface energy regions 11 and 12 with a narrow high surface energy region 10. This region is not filled with conducting material. During the drying of the semiconducting ink the entire contact line is located in a region of high surface energy, and dewetting is prevented. The design in Fig. 3C allows to minimize the surplus area of the active layer island extending beyond the area of the conducting electrodes.

Another important requirement for fabrication of high performance devices is the drying profile of the semiconducting ink material. It is desirable that the thickness of the semiconducting active layer island that is typically on the order of 10-100nm is as homogeneous as possible over the dimension of the device (Fig. 5A). In some cases after being repelled by the high surface energy region 11, the semiconducting ink droplet might further recede before drying with a contact line no longer in contact with the boundary between regions 13 and 11 (Fig. 5B). This

is not problematic as long as the film remains sufficiently thin and continuous the region of the active channel, and remains in contact with both the source and drain electrodes.

However, more commonly in the case of low surface tension inks the ink tends to dry in a coffee-stain drying mode, where the contact line becomes pinned at the boundary of region 11 and 13, and a flow of liquid and material towards the edge of the droplet is established. This flow is driven by the higher rate of liquid evaporation near the edge of the droplet than in its centre. Material is therefore deposited preferentially at the edges of the droplet (Fig. 5C). In most cases, this is undesirable, as it results in very thin, and possibly discontinuous films in the active channel region of the device. It also increases the tendency of the droplets to dewet from the very thin central region 10.

Coffee-stain drying can be prevented by increasing the viscosity of the solution, by reducing the evaporation time, for example by using lower boiling point solvents, deposition at elevated temperature, exposing the substrate to electromagnetic radiation during deposition and drying, or by flowing a stream of "dry" inert gas over the substrate during deposition. In this way a highly viscous solution state is reached more quickly before all the material has flown to the edges of the droplet.

After deposition of the semiconducting active laser island, the devices are completed by deposition of a gate dielectric layer with a thickness of typically 50 nm to 2000 nm and a conducting gate electrode. As mentioned above the gate dielectric may either be in the form of a continuous layer (fabricated by techniques such as spin coating, spray or blade coating), which then requires via-hole interconnections in many application, or in the form of a patterned active layer island. In the latter case several cases are possible. Preferably, the deposition of the dielectric island extends a certain distance beyond the semiconducting active

layer island, at least in regions where the gate interconnect 18 is printed over the edge of the dielectric island (Fig. 5(A)).

Formation of a continuous gate dielectric layer, or of the device configuration in Fig. 5(A) requires that the dielectric ink is not strongly repelled from surface region 11. This can be achieved by treating the substrate prior to deposition of the dielectric solution to increase wetting in region 11. Alternatively, interleaved printing can be used, such that a few isolated droplets are deposited first into region 11 without coming in contact with the lower surface energy regions of the device. Once these droplets have dried they provide anchoring points which allow printing of a continuous dielectric layer covering the active device area and adjacent boundary regions in region 11. As a further alternative printing from a high viscosity solution favours the formation of continuous films on top of low energy surface substrates. In techniques such as inkjet printing the maximum solution viscosity is limited to typically 20-40 cpi, but with techniques such as screen printing even higher viscosity formulations can be deposited.

An alternative configuration is shown in Fig. 5B, that is observed often for highly fluorinated surface energy barriers. In this case the dielectric ink is strongly repelled by surface region 11, and its deposition is confined to the active layer island. In this case it is possible to avoid electrical shorts between the gate interconnects printed over the edge of the dielectric island and one of the source and drain electrodes if region 10 is not filled completely filled with conducting material such as for example in the device configurations shown in Fig. 3(B) and (C). Alternatively a separate dielectric material 19 (Fig. 5(C)) can be deposited over the edge of the dielectric island to prevent electrical shorting and reduce leakage currents.

According to one embodiment of the invention a 50 nm thick film of polyimide is deposited on top of a 1737 glass substrate. The polyimide film is patterned by

photolithography, followed by oxygen plasma etching to expose the bare glass substrate in surface region 10. Typical lateral dimension of region 12 are L =0.1 - 10 μm, the width of region 10 is typically on the order of 20-60 μm. Then the substrate is exposed to a CF_4 plasma treatment (50-100 W for 5 min), during which the hydrophobic polyimide bank regions 11 and 12 are fluorinated. Subsequently, source-drain electrode are formed by inkjet printing PEDOT/PSS droplets into region 10 and/or on top of region 12. Then an ink of the semiconducting polymer poly(dioctylfluorene-co-bithiophene) formulated in a 0.25 % solution by weight in m-xylene or a 0.25 % solution by weight of a 3:1 mixture of m-xylene and cyclohexylbenzene is inkjet printed on top of region 12. The pure xylene ink is drying more quickly than the solvent mixture ink, the solvent mixture ink has a higher viscosity than the pure xylene ink. The ink is repelled from region 11, but it does not dewet on top of region 12. After deposition the semiconducting ink is dried in a vacuum oven for 3 hours. Then a 700-1300 nm thick film of polymethylmethacrylate in butylacetate is deposited by spin coating at a speed of 2000 rpm. The surface of the PMMA is then made wetting by a short O_2 plasma exposure (50W, 30s), and a gate electrode of PEDOT/PSS is inkjet printed on top.

The processes and devices described herein are not limited to devices fabricated with solution-processed polymers. Some of the conducting electrodes of the TFT and/or the interconnects in a circuit or display device (see below) may be formed from inorganic conductors, that can, for example, be deposited by printing of a colloidal suspension or by electroplating onto a pre-patterned substrate. In devices in which not all layers are to be deposited from solution one or more PEDOT/PSS portions of the device may be replaced with an insoluble conductive material such as a vacuum-deposited conductor.

For the semiconducting layer any solution processible conjugated polymeric or oligomeric material that exhibits adequate field-effect mobilities exceeding 10^{-3} cm^2/Vs, preferably exceeding 10^{-2} cm^2/Vs, may be used. Suitable materials are

reviewed for example in H.E. Katz, J. Mater. Chem. 7, 369 (1997), or Z. Bao, Advanced Materials 12, 227 (2000). Other possibilities include small conjugated molecules with solubilising side chains (J.G. Laquindanum, et al., J. Am. Chem. Soc. 120, 664 (1998)), semiconducting organic-inorganic hybrid materials self-assembled from solution (C.R. Kagan, et al., Science 286, 946 (1999)), or solution-deposited inorganic semiconductors such as CdSe nanoparticles (B. A. Ridley, et al., Science 286, 746 (1999)).

The electrodes may be coarse-patterned by techniques other than inkjet printing. Suitable techniques include soft lithographic printing (J.A. Rogers et al., Appl. Phys. Lett. 75, 1010 (1999); S. Brittain et al., Physics World May 1998, p. 31), screen printing (Z. Bao, et al., Chem. Mat. 9, 12999 (1997)), and photolithographic patterning (see WO 99/10939), offset printing, flexographic printing or other graphic arts printing techniques. Ink-jet printing is considered to be particularly suitable for large area patterning with good registration, in particular for flexible plastic substrates.

Although preferably all layers and components of the device and circuit are deposited and patterned by solution processing and printing techniques, one or more components may also be deposited by vacuum deposition techniques and/or patterned by a photolithographic process.

Devices such as TFTs fabricated as described above may be part of a more complex circuit or device in which one or more such devices can be integrated with each other and or with other devices. Examples of applications include logic circuits and active matrix circuitry for a display or a memory device, or a user-defined gate array circuit.

The patterning process may be used to pattern other components of such circuit as well, such as interconnects, resistors, capacitors etc.

The present invention is not limited to the foregoing examples. Aspects of the present invention include all novel and/or inventive aspects of the concepts described herein and all novel and/or inventive combinations of the features described herein.

The applicant hereby discloses in isolation each individual feature described herein and any combination of two or more such features, to the extent that such features or combinations are capable of being carried out based on the present specification as a whole in the light of the common general knowledge of a person skilled in the art, irrespective of whether such features or combinations of features solve any problems disclosed herein, and without limitation to the scope of the claims. The applicant indicates that aspects of the present invention may consist of any such individual feature or combination of features. In view of the foregoing description it will be evident to a person skilled in the art that various modifications may be made within the scope of the invention.

CLAIMS

1. A method for forming on a substrate an electronic device including at least one electrically conductive material and one semiconductive material deposited onto the substrate from liquid mixtures, the method comprising:

forming on the substrate a confinement structure including a first zone in a first area of the substrate, a second zone in a second area of the substrate, a third zone in a third area of the substrate, and a fourth zone in a fourth area of the substrate spaced from the second area by the third area,

the first, and third zone having a greater repellence for the mixture of the conductive material than the second and fourth zone,

depositing the electrically conductive material on the substrate by applying the electrically conductive mixture over the substrate,

depositing the semiconductive material on the substrate by applying the semiconductive mixture over the substrate,

whereby the electrically conductive material is confined by the relative repellence of the first and third zone to the spaced-apart second and fourth areas, and the semiconductive mixture is confined by the relative repellence of the first area to the second, third and fourth areas.

2. A method as claimed in claim 1 wherein the semiconductive material only covers the second and fourth area partially.

3. A method as claimed in claim 1 to 2, comprising the additional step of depositing at least one further material on top of the conductive and semiconductive material.

4. A method as claimed in claim 3, wherein said further material is deposited from solution.

5. A method as claimed in claim 1 to 4, wherein the width of the third zone between the second and fourth zone is less than 20 microns.

6. A method as claimed in claim 1 to 5, wherein the width of the third zone between the second and fourth zone is less than 1 microns.

7. A method as claimed in claim any preceding claim, wherein the electrically conductive material formed in the second and fourth zone forms source and drain electrodes of a transistor.

8. A method as claimed in any preceding claim, wherein the semiconductive material formed in the second, third and fourth zone is the active semiconducting island of a transistor.

9. A method as claimed in any preceding claim, wherein the surface of the substrate is surface treated in at least one of the first and third zones.

10. A method as claimed in any of claims 1 to 9, wherein the surface of the substrate in the first zone contains fluorinated species.

11. A method as claimed in claim 10, wherein the surface of the substrate in the first zone is fluorinated by exposure to a plasma treatment.

12. A method as claimed in claim 11, wherein the surface of the substrate in the first zone is fluorinated by exposure to a CF_4 plasma treatment.

13. A method as claimed in claim 10, wherein the surface of the substrate in the first zone is fluorinated by exposure to a fluorinated self-assembling monolayer molecule.

14. A method as claimed in any preceding claim, wherein the surface of the first and third zone are of essentially identical composition.

15. A method as claimed in any preceding claim, wherein the first and third zones are formed on the exposed surface of a layer deposited on a planar structural member.

16. A method as claimed in any preceding claim, wherein the surface of the substrate has a higher surface roughness in the first zone than in the second and fourth zone.

17. A method as claimed in any preceding claim, wherein the viscosity of the semiconductive mixture is higher than 5 cpi.

18. A method as claimed in any preceding claim, where in the boiling point of the semiconductive mixture is less than 180 °C.

19. A method as claimed in any preceding claim, wherein the semiconductive mixture is deposited onto a substrate held at a temperature higher than 40°C.

20. A method as claimed in any of claims 1 to 19, wherein the temperature of the semiconductive mixture is less than 20°C.

21. A method as claimed in any preceding claim, wherein a flow of gas is directed onto the substrate surface during the deposition of the semiconductive material.

22. A method as claimed in any preceding claim wherein the first zone and the third zone are not in contact with each other, but separated by a zone of lower repellence for the mixture of the semiconductive material.

23. A method as claimed in claim 22, wherein said zone of lower repellence for the mixture of the semiconductive material is not filled by the conductive material.

24. A method as claimed in claim 22 or 23 wherein said zone of lower repellence for the mixture of the semiconductive material is part of the second or the fourth zone.

25. A method as claimed in any preceding claim, wherein the contact angle difference of the semiconductive mixture on the surface of the third zone, is larger by more than 10° than its contact angle on the surface of the conductive material in the second and fourth zone.

26. A method as claimed in claim 25, wherein the contact angle difference of the semiconductive mixture on the surface of the third zone, is larger by more than 30° than its contact angle on the surface of the conductive material in the second and fourth zone.

27. A method as claimed in any preceding claim, wherein the contact angle of the semiconductive mixture on the surface of the third zone is smaller than 100°.

28. A method as claimed claim 27, wherein the contact angle of the semiconductive mixture on the surface of the third zone is smaller than 60°.

29. A method as claimed in any preceding claim, wherein said electrically conductive or semiconductive material is deposited by droplet deposition.

30. A method as claimed in any preceding claim, wherein said electrically conductive or semiconductive material is deposited by ink-jet printing.

31. A method as claimed in any preceding claim wherein said electrically conductive material is a polymer.

32. A method as claimed in any of claims 31, wherein said electrically conductive material is a conducting polymer.

33. A method as claimed in any of claims 1 to 31, wherein the electrically conductive material is an inorganic particulate material capable of suspension in the said liquid.

34. A method as claimed in any preceding claim, wherein the semiconductive material is a conjugated organic molecule.

35. A method as claimed in claim 34, wherein the semiconductive material is a conjugated polymer.

36. A method for forming an electronic device including at least one electrically conductive and one semiconductive material deposited onto the substrate from liquid mixtures, the method comprising: forming on the substrate a confinement structure including a first zone and a second zone, depositing the electrically conductive material on the substrate, wherein the electrically conductive material is absent from both the first and second zone, and subsequently depositing the electrically semiconductive material from solution, wherein the semiconductive material is absent from the first zone, but not from the second zone.

37. A logic circuit, display, sensor or memory device formed by the method of any preceding claim.

38. A logic circuit, display, sensor or memory device comprising a plurality of transistors formed by the method of any preceding claim.

ABSTRACT

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A method for forming an electronic device including at least one electrically conductive and one semiconductive material deposited from solution, the method comprising: forming on the substrate a confinement structure consisting of a least a first zone and a second zone, depositing the electrically conductive material on the substrate, wherein the electrically conductive material is absent from both the first and second zone, and subsequently depositing the electrically semiconductive material from solution, wherein the semiconductive material is absent from the first zone, but not from the second zone.

Figure 1

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